



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,888	02/01/2001	Jun Koyama	740756-2255	3194
22204	7590	10/19/2004	EXAMINER	
NIXON PEABODY, LLP 401 9TH STREET, NW SUITE 900 WASHINGTON, DC 20004-2128			WEISS, HOWARD	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/774,888

Applicant(s)

KOYAMA ET AL.

Examiner

Howard Weiss

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1 and 75-101 ~~is~~ are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 75-101 ~~is~~ are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

Attorney's Docket Number: 740756-2255

Filing Date: 2/1/01

Continuing Data: RCE established 3/27/03, 8/19/04

Claimed Foreign Priority Date: 2/1/00 (JPX)

Applicant(s): Koyama et al. (Kato)

Examiner: Howard Weiss

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/19/04 has been entered.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
3. Claims 75, 76, 85, 86, 91 and 92 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama (U.S. Patent No. 5,793,344).

Koyama shows all aspects of the instant invention (e.g. Figure1) including:

- a semiconductor device **110** on a substrate (not shown; Column 3 Line 57)
- a non-volatile memory **115** over the substrate
- a pixel portion **111** over the substrate
- a source wiring driver circuit **113** for driving the pixel portion over the substrate
- a gate wiring driver circuit **112** for driving the pixel portion over the substrate
- a correction circuit **116** over the substrate

- a memory controller circuit **114** over the substrate for controlling the non-volatile memory circuit
- the device part of an LCD of a video camera

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (JP 11-154714 and the Derwent Translation of this document) and Akbar (U.S. Patent No. 5,656,845).

Yamazaki et al. show most aspects of the instant invention (e.g. Figures 1, 2 and 8) including:

- a memory cell array with memory cells formed in a matrix
- each cell containing a memory thin film transistor (MTFT) **Tr1** and a switching thin film transistor (STFT) **Tr2** said transistors integrally formed (Paragraph 0011 of Derwent)

- said MTFT including:
  - a first semiconductor active layer **202** formed on an insulating substrate **201** and having a first thickness **d1**
  - a first insulating film **211**, a floating gate electrode **213**, a second insulating film **214** and a control gate electrode **215**
  - a wiring **825** for connecting the control gate to a first single line **809**
- said STFT including:
  - a second semiconductor active layer **206** formed on an insulating substrate **201** and having a second thickness **d2**
  - a gate insulating layer **212** and a gate electrode **217**
  - a second signal line **810** connected to said gate electrode
- where in **d1** is thinner (i.e. smaller) than **d2** and within the ranges claimed (Paragraphs 0058 and 0059)
- the floating gate comprising tantalum or tantalum and the second insulating film made of a thermal oxide of said floating gate (i.e. tantalum oxide; Paragraphs 0149 to 0153)

Yamazaki et al. does not show the first and second semiconductor layer in a common semiconductor island. Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a common semiconductor island (i.e. layer) **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a common semiconductor island as taught by Akbar in the device of Yamazaki et al. to provide memory cells with improved performance and reliability.

6. Claims 77 to 84, 97 to 90 and 93 to 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. and Akbar, as applied to claims 75 and 76 above, and further in view of Koyama.

Yamazaki et al. and Akbar show most aspects of the instant invention (Paragraph 5) except for the semiconductor device comprising a substrate, a non-volatile memory over the substrate, a pixel portion over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate, a gate wiring driver circuit for driving the pixel portion over the substrate, a correction circuit over the substrate and a memory controller circuit over the substrate for controlling the non-volatile memory circuit all part of an LCD of a video camera. Koyama teach (Paragraph 3) to use the memory device with the listed devices to produce a high quality display device (Column 7 Lines 55 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to use the memory device of Yamazaki et al. and Akbar with the listed devices of Koyama to produce a high quality display device.

7. Claims 97 to 101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., Akbar and Koyama, as applied to Claims 1, 77, 78, 79 and 80 above, and further in view of Fukaya et al. (U.S. Patent No. 5,627,088).

Yamazaki et al., Akbar and Koyama show most aspects of the instant invention (Paragraph 6) except for the use of amorphous silicon germanium. Fukaya et al. teach (e.g. Column 11 Lines 8 to 10) to use amorphous silicon germanium as a semiconductor layer in an LCD device to provide an alternative semiconductor material. It would have been obvious to a person of ordinary skill in the art at the time of invention to use amorphous silicon germanium as a semiconductor layer in an LCD device as taught by Fukaya et al. in the device of Yamazaki et al., Akbar and Koyama to provide an alternative semiconductor material.

### ***Double Patenting***

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759

F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1 and 75 to 96 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 to 12 of U.S. Patent No. 6,472,684 in view of Akbar, Yamazaki et al. and Koyama. U.S. Patent No. 6,472,684 claim most aspects of the instant except for the first and second semiconductor layer a common semiconductor island, the floating gate comprising tantalum, the second insulating film comprising a thermal oxide of said floating gate and being part of the listed elements (i.e. a substrate, a non-volatile memory over the substrate, a pixel portion over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate, a gate wiring driver circuit for driving the pixel portion over the substrate, a correction circuit over the substrate and a memory controller circuit over the substrate for controlling the non-volatile memory circuit all part of an LCD of a video camera).

Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a continuous layer **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). Yamazaki et al. teach (e.g. Paragraphs 0149 to 0153)) to use tantalum in the floating gate and a thermal oxide of the floating gate as the second insulating film to improve the electrical characteristics of the device. Koyama teach (Paragraph 2) to use the memory device with the listed devices to produce a high quality display device (Column 7 Lines 55 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to

form first and second semiconductor layers in a continuous layer as taught by Akbar, to use tantalum in the floating gate and a thermal oxide of the floating gate as the second insulating film as taught by Yamazaki et al. and to use the memory device with the listed devices as taught by Koyama in the device claimed in U.S. Patent No. 6,472,684 to provide a device with improved performance and reliability.

10. Claims 1 and 75 to 96 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1 to 30 of U.S. Patent No. 6,509,602 in view of Akbar, Yamazaki et al. and Koyama. U.S. Patent No. 6,509,602 claim most aspects of the instant except for the first and second semiconductor layer a common semiconductor island, the floating gate comprising tantalum, the second insulating film comprising a thermal oxide of said floating gate and being part of the listed elements (i.e. a substrate, a non-volatile memory over the substrate, a pixel portion over the substrate, a source wiring driver circuit for driving the pixel portion over the substrate, a gate wiring driver circuit for driving the pixel portion over the substrate, a correction circuit over the substrate and a memory controller circuit over the substrate for controlling the non-volatile memory circuit all part of an LCD of a video camera).

Akbar teaches (e.g. Figures 1, 9 and 10) to form first and second semiconductor layers in a continuous layer **122** to provide memory cells with improved performance and reliability (Column 2 Lines 19 to 22). Yamazaki et al. teach (e.g. Paragraphs 0149 to 0153)) to use tantalum in the floating gate and a thermal oxide of the floating gate as the second insulating film to improve the electrical characteristics of the device. Koyama teach (Paragraph 2) to use the memory device with the listed devices to produce a high quality display device (Column 7 Lines 55 to 61). It would have been obvious to a person of ordinary skill in the art at the time of invention to form first and second semiconductor layers in a continuous layer as taught by Akbar, to use tantalum in the floating gate and a thermal oxide of the floating gate as the second insulating film as taught by Yamazaki et al. and to use the memory device



with the listed devices as taught by Koyama in the device claimed in U.S. Patent No. 6,509,602 to provide a device with improved performance and reliability.

### ***Response to Arguments***

11. Applicant's arguments filed 8/19/04 have been fully considered but they are not persuasive. The Applicants state that since Kayama only states but does not show the LCD device formed on a substrate, the Examiner could not conclude that Kayama anticipates an LCD device on a substrate as claimed. However, Kayama clearly includes the substrate with the LCD device but does not explicitly show the substrate for simplicity. The device of Kayama could not function without the substrate in place. Additionally, the LCD device is feature **110** and this been corrected in the present rejection. In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

### ***Conclusion***

12. Paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

13. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice

Art Unit: 2814

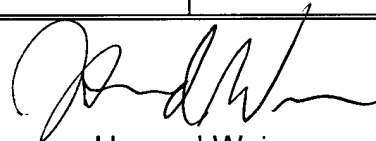
---

published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**.

15. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/326, 347; 365/ 185.05	thru 10/15/04
Other Documentation: none	
Electronic Database(s): EAST	thru 10/15/04



Howard Weiss  
Patent Examiner  
Art Unit 2814

HW/hw  
18 October 2004